AMENDMENTS TO THE CLAIMS

This listing of claims of claims will replace all prior versions, and listings, of claims in the Application:

LISTING OF CLAIMS:

Claims 1 – 5 (Canceled).

Claim 6 (Currently Amended) A method for debugging ~~, implemented~~ in a computer system~~,~~ including a central processing unit connected to a North-bridge chipset and a South-bridge chipset, said method comprising:

~~Sending~~ sending a system management interrupt signal from said South-bridge chipset to said central processing unit, thereby triggering a debugging tool program;

executing said debugging tool program to pop out a debugging operation window ~~after~~ upon said central processing unit has entered a system management mode;

selecting, in said debugging operation window, and executing ~~each~~ at least one debugging item;

setting a trap address for said debugging operation window; and

~~Leaving~~ leaving the debugging operation window ~~after end of~~ upon the execution of said at least one debugging item has been accomplished;

~~Wherein~~ wherein, once the debugging tool program has been executed ~~finished the debugging execution~~, said central process unit ~~is able~~ returns to ~~execute~~ execution of a next queued instruction , and

wherein, after leaving said debugging operation window upon the execution of said at least one debugging item has been accomplished, said debugging operation window is popped out repeatedly from said trap address each time when said South-bridge chipset is triggered .

Claim 7 (Currently Amended) The method of claim 6, wherein said at least one debugging item ~~comprises~~ is selected from a group consisting of access input and output, access memory, access device configuration and trap set for specific IO address.

Claim 8 (Original) The method of claim 6, wherein said debugging operation window is programmable.

Claim 9 (Currently Amended) The method of claim 6, wherein before the step of said South-bridge chipset sending said system management interrupt signal to said central processing unit, said South-bridge chipset is triggered by users through a predetermined general purpose input/output pin.

Claims 10 – 11 (Canceled).

Claim 12 (Currently Amended) A device for debugging, ~~which comprises~~ comprising:

a central processing unit; ~~and~~

a South-bridge chipset and a North-bridge chipset connected to said central processing unit, said South-bridge chipset including a system management interrupt pin for sending system management interrupt signal to said central processing unit, and a plurality of general purpose input/output pins for being triggered; ~~used to trigger by users~~

a debugging operation window having a predetermining trap address; and

a unit retrieving said debugging operation window from said

predetermined trap address each time said general purpose input/output pins of said South-bridge chipset are triggered.

Claim 13 (Currently Amended) The device of claim 12, wherein said central processing unit is connected with at ~~lease~~ least one memory.

Claim 14 (Original) The device of claim 13, wherein said memory comprises a system management mode section.

Claim 15 (Original) The device of claim 14, wherein said system management mode section comprises a debugging tool program.

Claim 16 (Canceled).

Claim 17 (Currently Amended) The device of claim 12, wherein said system management interrupt signal is sent through said system management interrupt pin when said South-bridge chipset triggered ~~by users~~.

Claim 18 (Currently Amended) The device of claim 12, wherein said system management interrupt signal is sent through ~~the~~ links between said South-bridge and North-bridge chipsets and central processing unit when said South-bridge chipset is triggered ~~by users~~.

Claim 19 (Currently Amended) The device of claim ~~17~~ 15, wherein said system management interrupt signal enables said central processing unit to move into said system management mode section to execute said debugging tool program.

20. (Canceled).